Princess Sumaya University for Technology

King Abdullah II Faculty of Engineering

Electrical Engineering Department



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| **Full adder Using Glade** |

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***Abstract***

*In this project, a full-adder circuit is designed and constructed using the GLADE (Graphical Layout Editor) software. This circuit is made of CMOS AND, XOR, and OR gates. Moreover, it is considered an essential circuit for arithmetic units. Key phases in the design process include schematic capture, layout design, and verification using Layout Versus Schematic (LVS), Design Rule Check (DRC), and Layout Parameter Extraction (LPE). Also, the inverter from an earlier assignment is included in the project. Once this project is finished successfully, a complete, tested, and working full-adder layout will be shown.*

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# Introduction

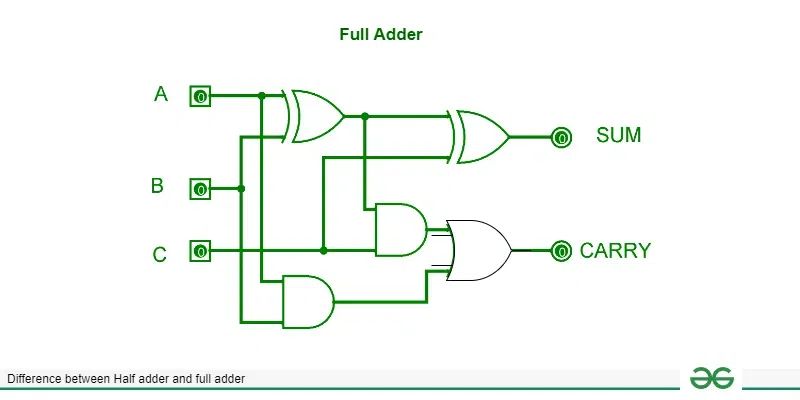
This report covers the design and implementation of a full-adder circuit employing GLADE software. A full-adder is a basic digital circuit that performs arithmetic addition on three one-bit inputs: two operands (A and B) and a carry-in. The circuit outputs two values: sum (S) and carry-out (Cout). 

Figure 1: Full adder structure.

The design process includes several stages. Individual logic gates (AND, OR, NOT, and XOR) will be created as both schematic and stick diagram representations. These representations are crucial for visualizing the circuit's structure to be able to conduct the layout. To ensure design integrity, verification will take place using Design Rule Checking (DRC), Layout Parameter Extraction (LPE), and Layout Versus Schematic (LVS).

These basic gates will be joined to form the complete adder circuit. The whole adder will be represented schematically as well as in layout. The final design will be thoroughly tested to ensure its functionality and performance.

# Design Principles

* The length of the transistor will be 30n.
* The ratio between the size of the PMOS AND NMOS is 8.
* The inverter used will have the ratio of 1.5 as it is used from a previous assignment.

# Procedure

## AND GATE

### Stick diagram:

Figure 2: Stick diagram of the Nand gate.

### Schematic:

A screenshot of a video game

Description automatically generated

Figure 3: The schematic representation of the AND gate.

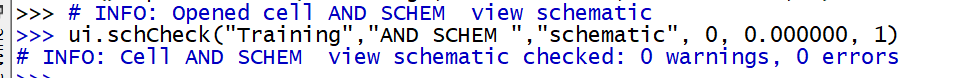


Figure 4: The result of checking the schematic of the AND gate.

### LAYOUT:

A blueprint of a building

Description automatically generated

Figure 5: The layout representation of the AND gate.

### TESTS:

DRC:

A black text on a white background

Description automatically generated

Figure 6: The results of running the DRC test on the AND gate.

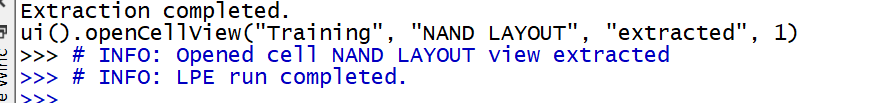
LPE: 

Figure 7:The results of running the LPE test on the AND gate.

LVE:

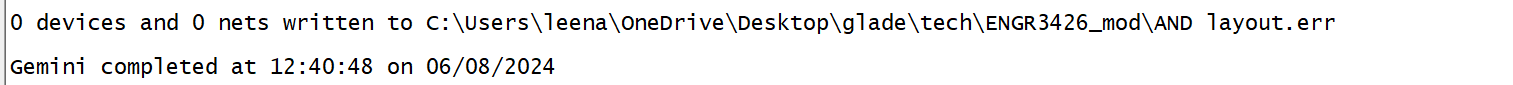


Figure 8: The results of running the LVS test on the AND gate.

## OR GATE

### Stick diagram:

A diagram of a circuit

Description automatically generated with medium confidence

### Schematic:

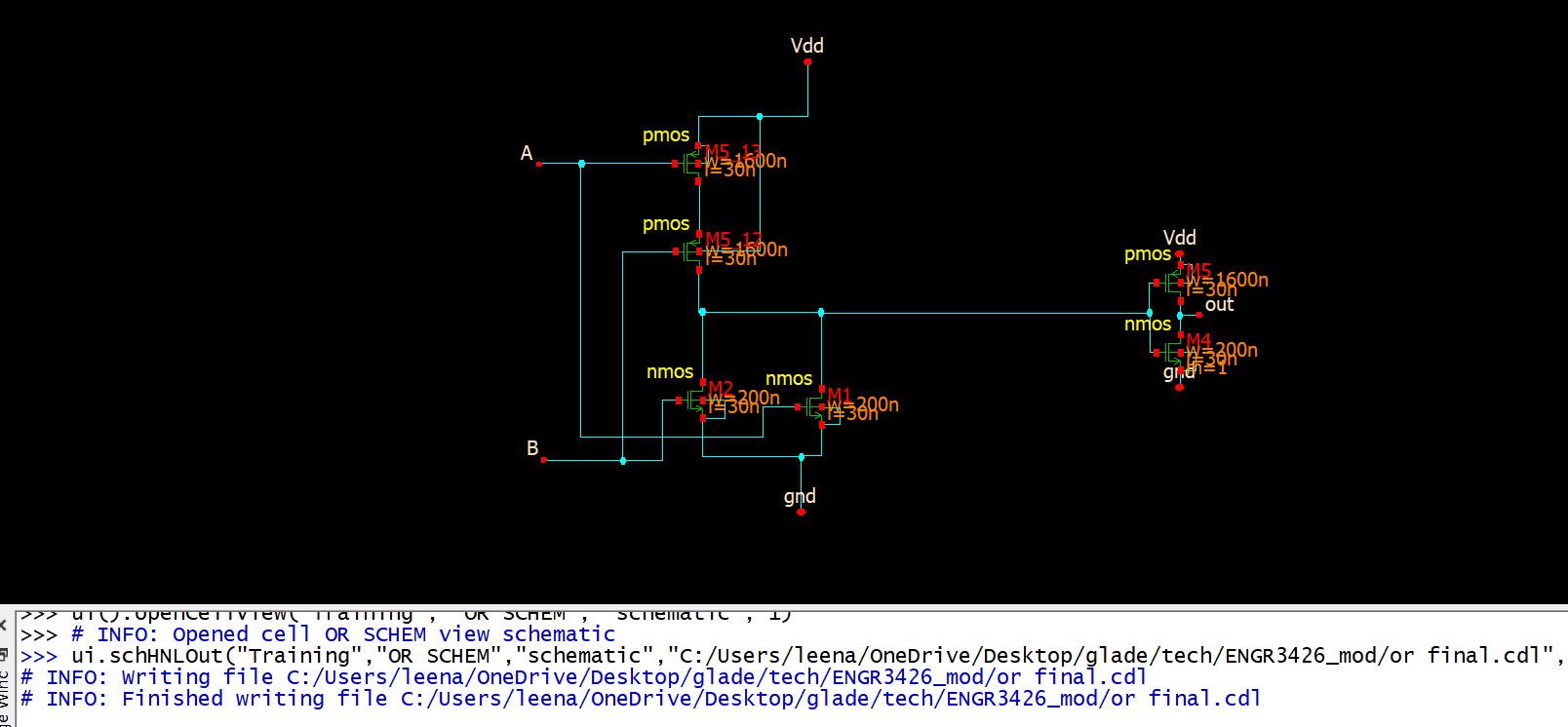


Figure 9 : The schematic representation of the OR gate.

### LAYOUT:

A diagram of a computer

Description automatically generated

Figure 10 : The layout representation of the OR gate.

### TESTS:

DRC:

A computer code with black text

Description automatically generated

Figure 11: The results of running the DRC test on the OR gate.

LPE:

A screenshot of a computer

Description automatically generated

Figure 12: The results of running the LPE test on the OR gate.

LVS: A computer screen shot of a building

Description automatically generated

Figure 13:The results of running the LVS test on the OR gate.

### XOR GATE

### Stick diagram: A grid with colored lines and text Description automatically generated with medium confidence

### A computer screen shot of a diagram Description automatically generatedSchematic

Figure 14: The schematic representation of the XOR gate.

### A computer screen shot of a diagram Description automatically generatedLAYOUT:

Figure 15: The layout representation of the XOR gate.

### TESTS:

DRC.

A screenshot of a computer code

Description automatically generated

Figure 16: The results of running the DRC test on the XOR gate.

LPE:

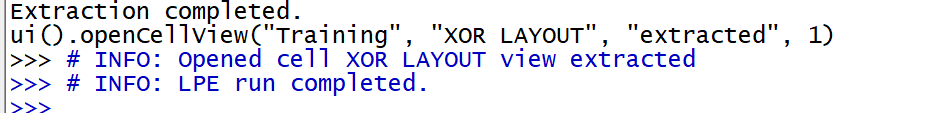


Figure 17: The results of running the LPE test on the OR gate.

LVS: A screen shot of a computer

Description automatically generated

Figure 18: The results of running the LVS test on the XOR gate.

# Full adder

After we ensure that all the gates are working properly we will connect them according to Figure 1 :

### Layout

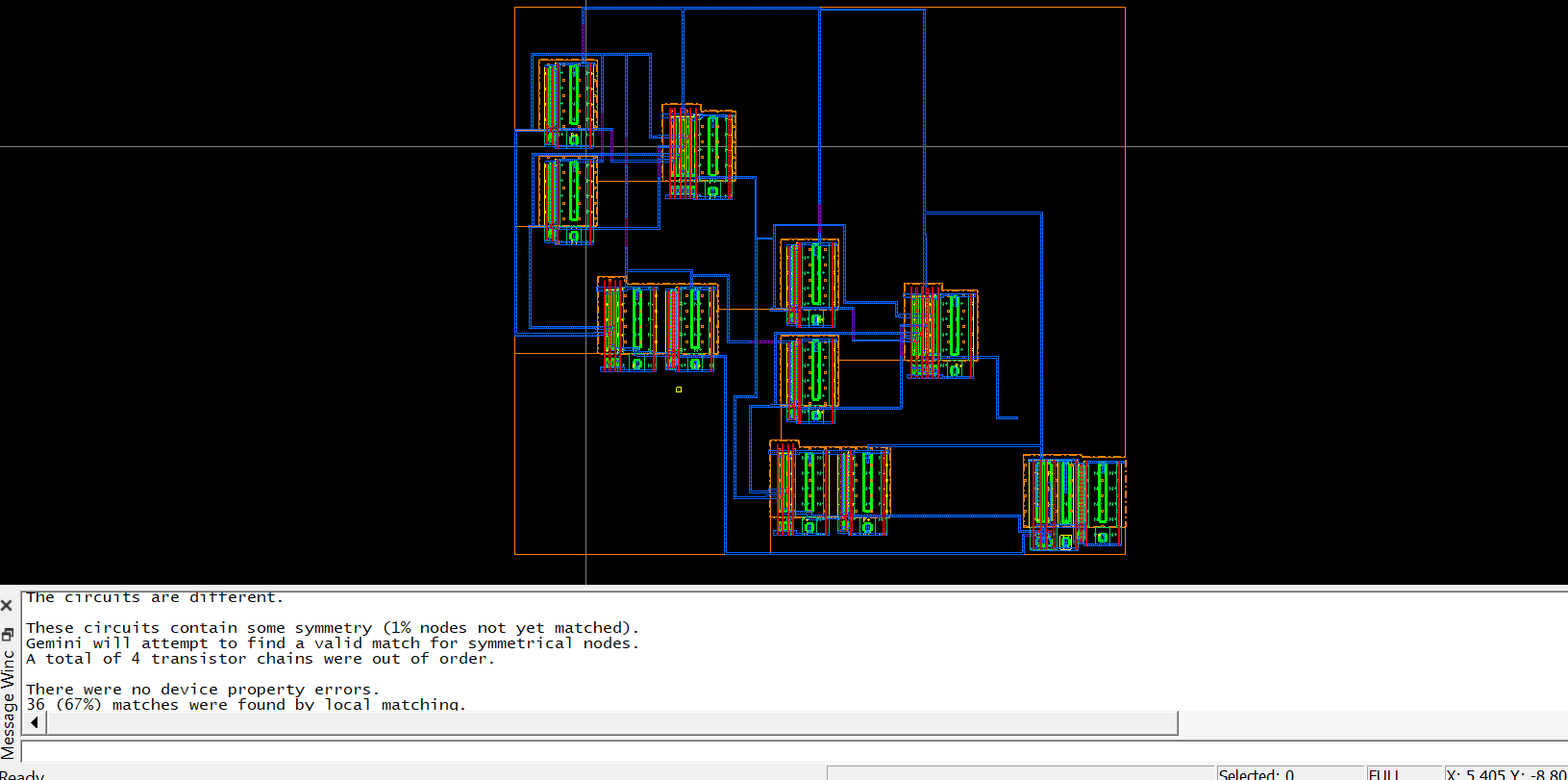


Figure 19: The Layout view of the full adder.

### Schematic

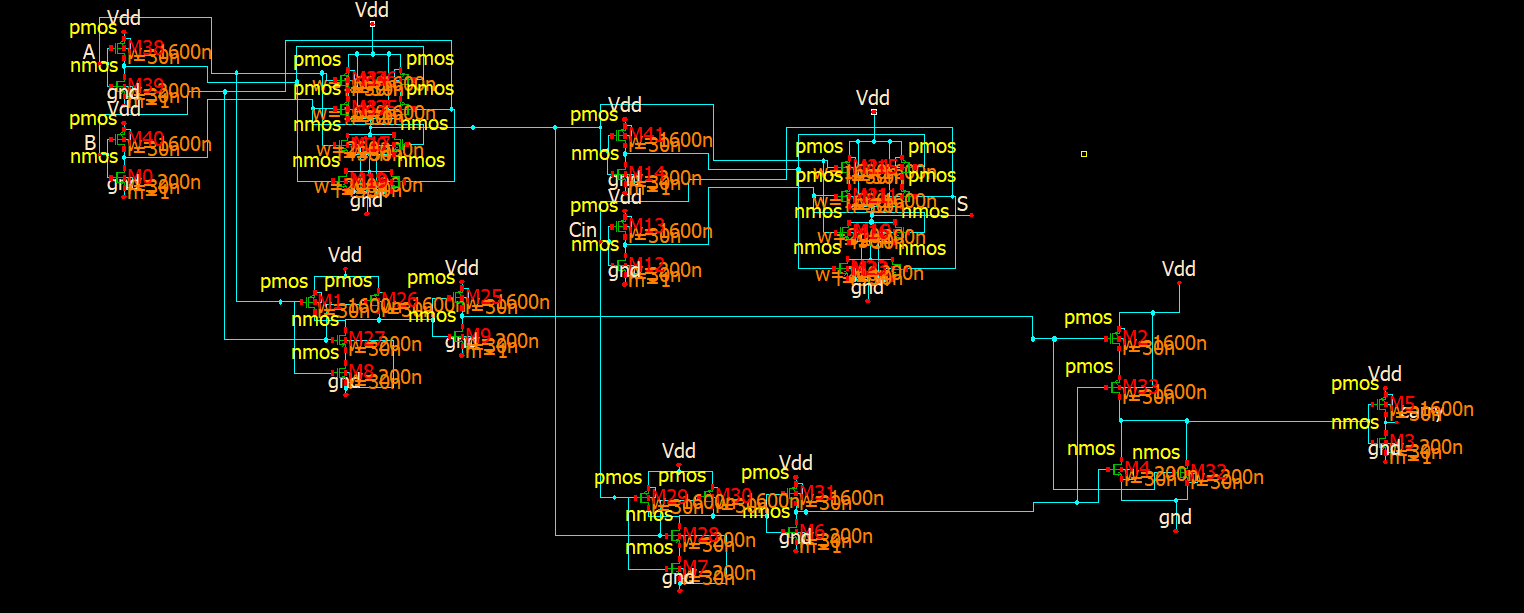


Figure 20: The schematic view of the full adder.

To check for the integrity of our design we run the 3 tests for the full adder:

DRC: 

Figure 21: The results of running the DRC test on the full adder gate.

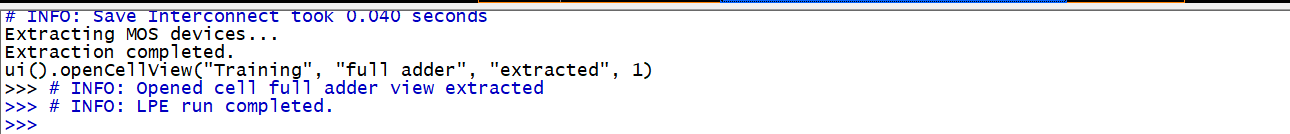
LPE: 

Figure 22: The results of running the LPE test on the full adder gate.

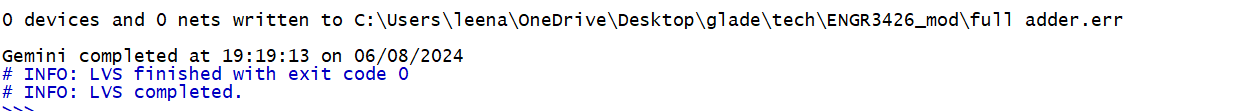
LVS: 

Figure 23: The results of running the LVS test on the full adder gate.

# Conclusion

In this report, we discussed the design and implementation of a full-adder circuit utilizing the GLADE program. The process started with the design of fundamental logic gates (AND, OR, NOT, and XOR) in schematic and stick diagram formats, which were later interconnected to make the full-adder circuit.

The design's accuracy and reliability were verified by extensive verification utilizing Design Rule Checking (DRC), Layout Parameter Extraction (LPE), and Layout Versus Schematic (LVS).   
  
This research demonstrated the ability to use GLADE software for designing and constructing digital circuits, providing useful insights into VLSI design techniques and verification methods.